Rail to Rail input and output amplifiers for Low-Voltage and Low-Power Implementations

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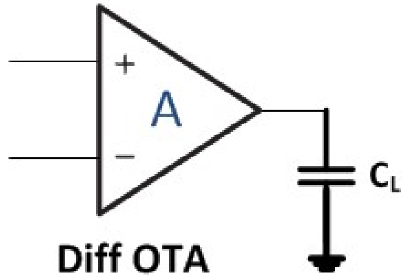
EPFL

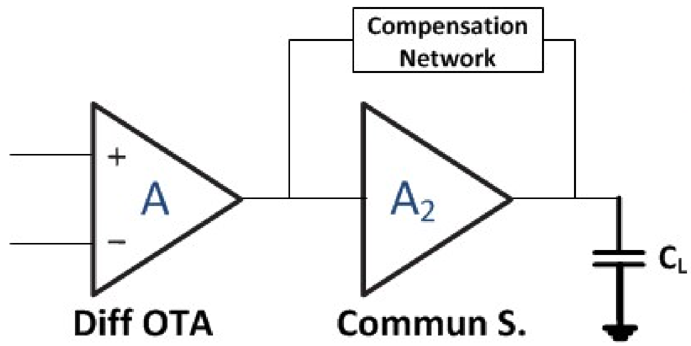
Rail to Rail in Single and Multistage Amps

One-stage



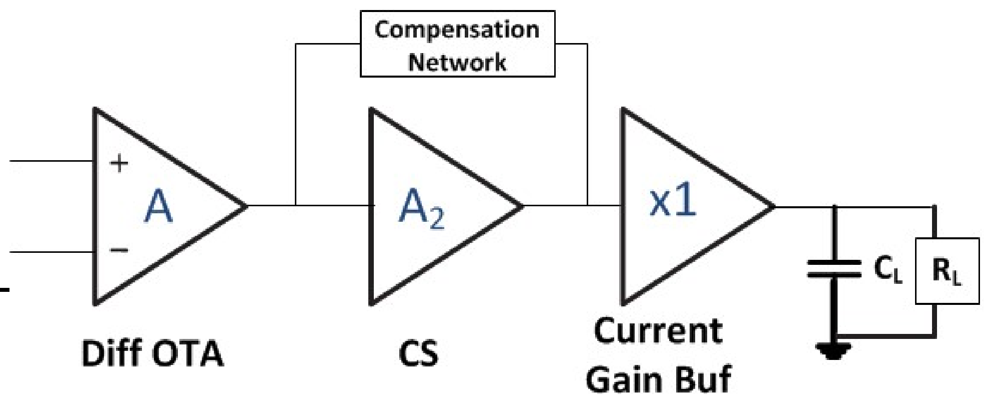
Gain boosting:
Cascode
Folded-Cascode
Auxiliary Amp.
Pb. Low swing

Two-stages



Compensation Tech. For stability
OTA for H. Gain
CS for H. Swing:

Three-stages



Current Gain Amplifier
Flower
Class AB

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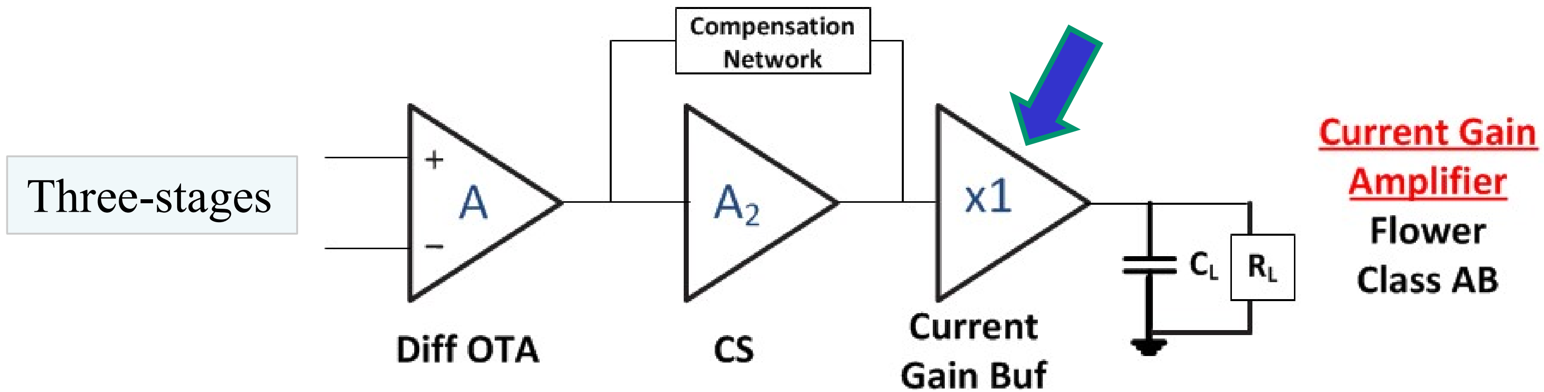
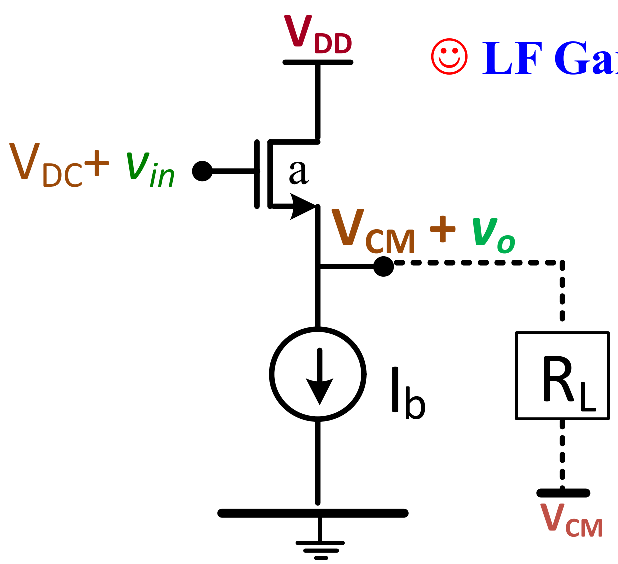
OA Output Buffer for low resistive load: Class A, B and AB



Source Follower in LV-LP implementations



☺ **LF Gain:** $A_o = \dfrac{g_{m,a}}{g_{m,a}+g_{ds,a}+g_{ds,b}+R_L{}^{-1}} \xrightarrow{R_L \gg 1/g_{m,a}} 1$

☺ **R_{out}:**

$$R_o \approx \frac{1}{g_{m,a}}$$

☺ **C_{in}:**

$$C_{in} \approx C_{GD}$$

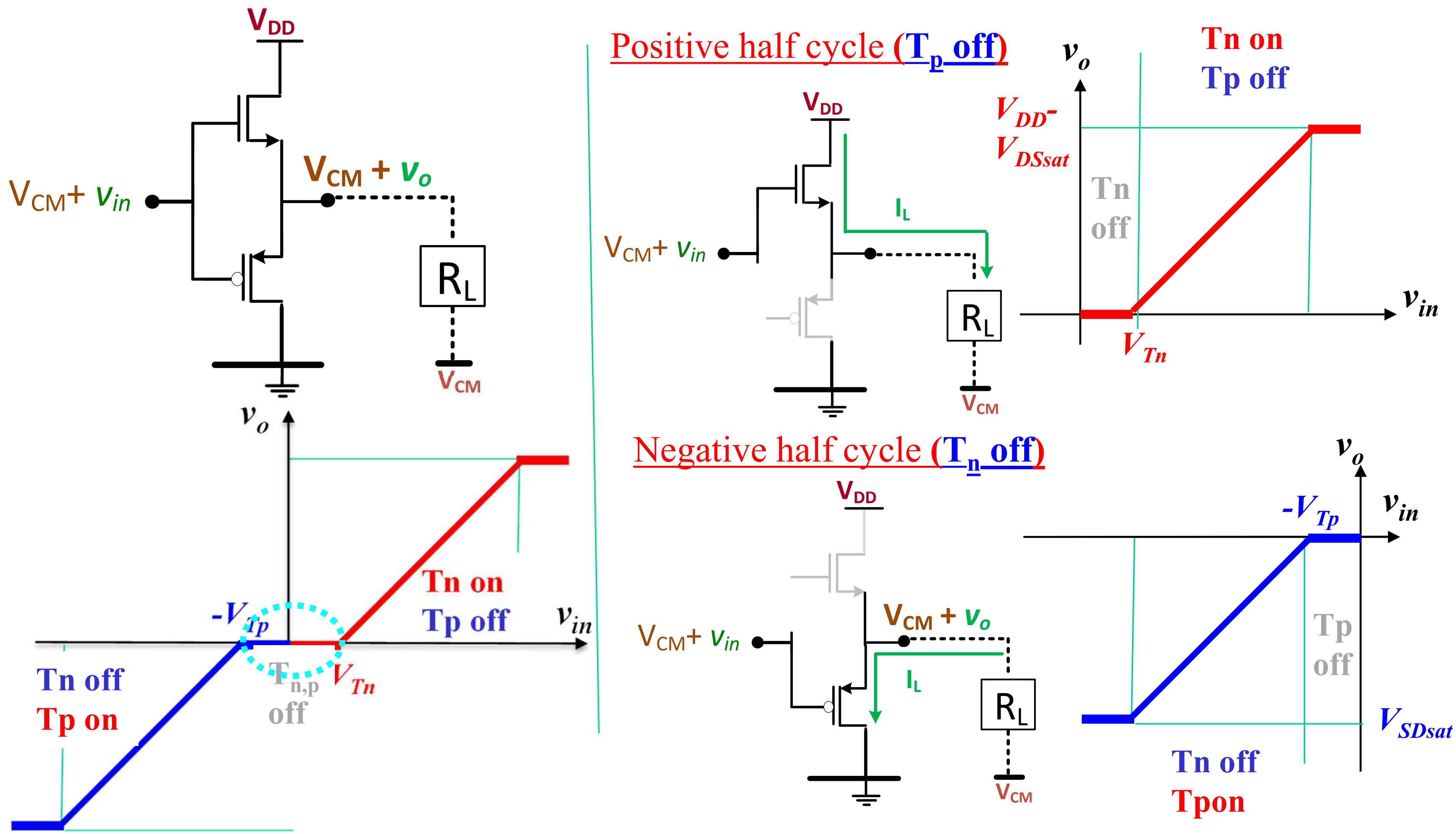
(no Miller effect because ΔVin ≈ ΔVo)

- $V_{inMaX} = V_{DD}$; $V_{inMin} = V_{GS} + V_{SDsatb}$
  Input swing = V_{DD} - $V_{GS} - V_{SDsatb}$
- Output swing = V_{DD} - $V_{GS} - V_{SDsatb}$ (☹ for LV)
  $\mathbf{v_{omax} = I_b R_L}$ (☹ ☹ for LP)

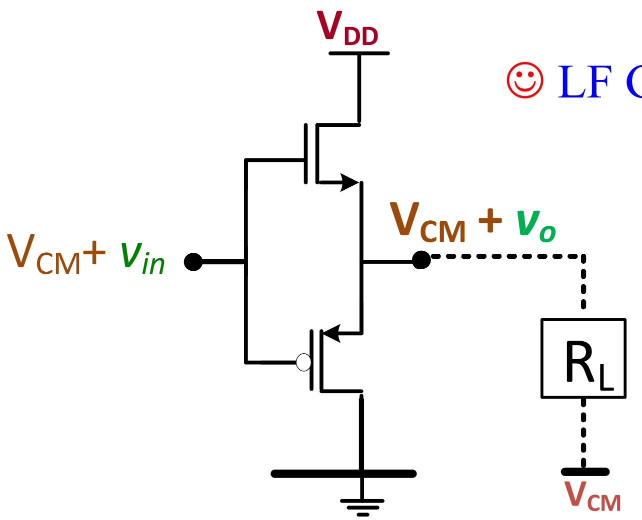
- Main drawback: Power consumption:
  - Ex: for R_L= 100 Ω and $\mathbf{v_o}$ **= 1V → $\mathbf{I_{bmin}}$ = 10 mA** 

    even in quiescent condition (Class A)

push-pull "source to source" follower: Class B



push-pull “source to source” follower: Class B

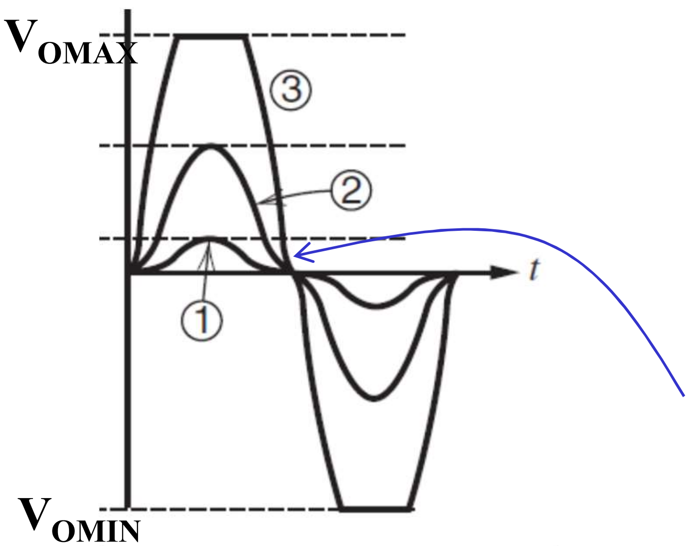


☺ LF Gain: $A_o \approx \dfrac{g_{m.n,p}}{g_{ds,n,p}+g_{m,n,p}+R_L{}^{-1}} \xrightarrow{\mathbf{R_L >> 1/g_{m,n,p}}} 1$

☺ R_{out}: $R_o \approx \dfrac{1}{g_{mn,p}}$

☺ C_{in}: $C_{in} \approx C_{GDn} + C_{GDp}$
(no Miller effect because ΔVin ≈ ΔVo)

- $V_{inMin} = V_{GSn} + V_{SDsatp} \approx V_{SDsatp}$
  $V_{inMaX} = V_{DD} - V_{DSsatn} - V_{SGp} \approx V_{DD} - V_{DSsatn}$
  Input swing $= V_{DD} - V_{DSsatn} - V_{SDsatp}$



- **Output swing ≈** $V_{DD} - V_{DSsatn} - V_{SDsatp}$ (~rail to rail ☺ for LV)
- **Class B no current in the quiescent condition** (☺ for LP)
- **Crossover distortion when the two transistors are off** (Linearity issu ☹)

→ **solution class AB**

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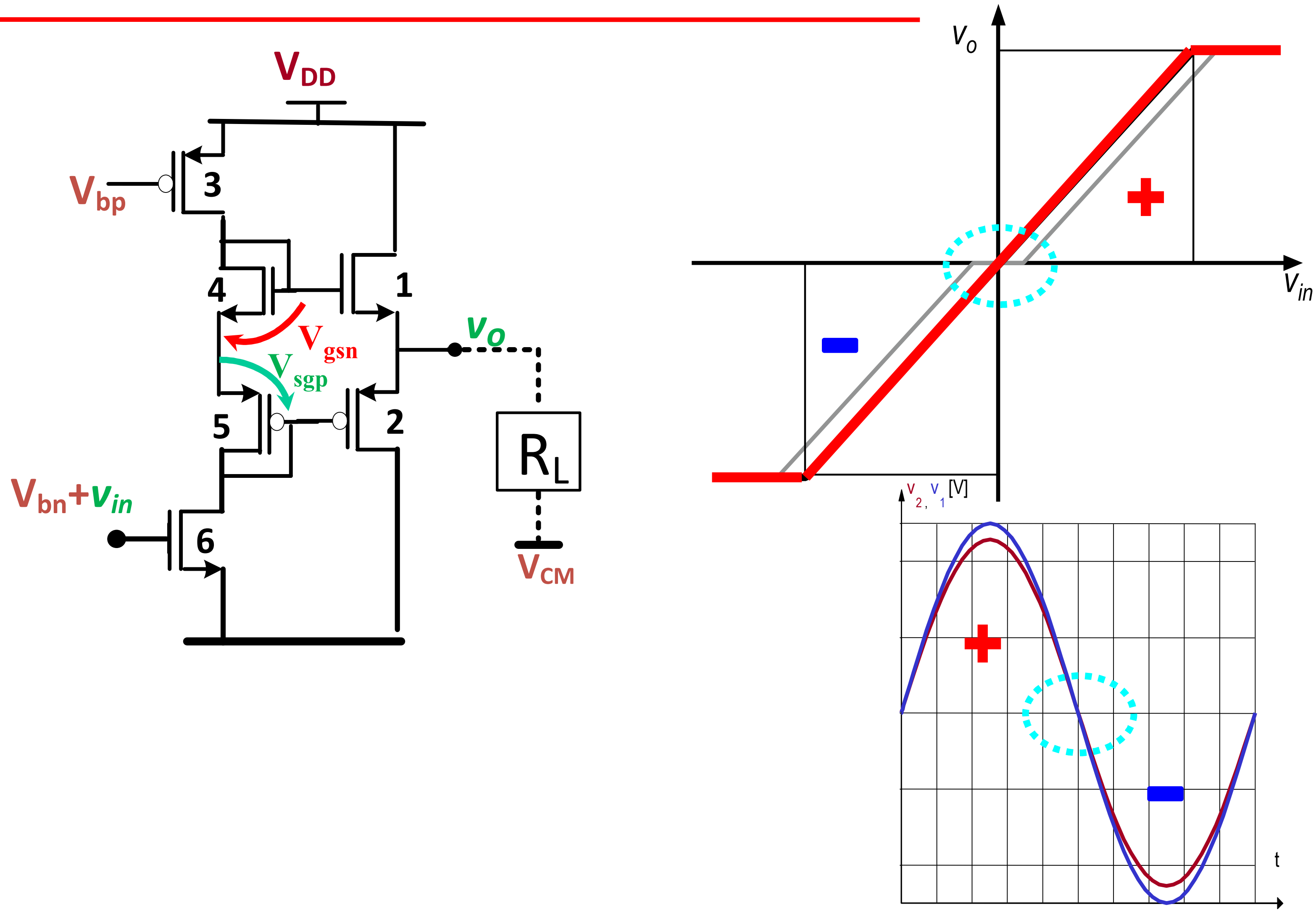
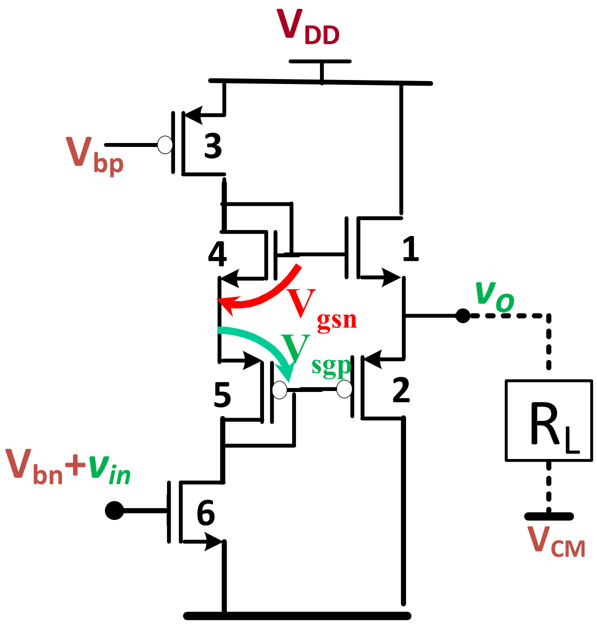
push-pull source-follower: Class AB



push-pull source-follower: Class AB



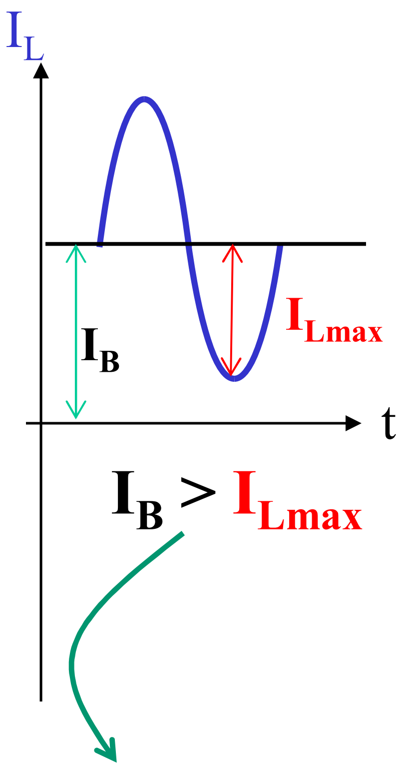
- Transistors 4 and 5 act like a floating voltage source. 3 is a current source, so the voltage across 4 and 5 is constant.
- 6 forms a common-source stage that allows moving the floating voltage source up and down. This eliminates the region where neither M1 nor M2 is conducting. Therefore crossover distortion is reduced. (☺☺ for Linearity)
- The dimensioning is usually done for **the quiescent condition** where the output signal is zero. For this case 4/1 and 5/2 act like current mirrors. The ratio determines the quiescent current.

$$A_o \approx -\frac{g_{m6}}{g_{ds6}+g_{ds3}} \qquad R_o \approx \frac{1}{g_{mn}+g_{mp}}$$

- **Small quiescent current I_B and no crossover distortion** (☺ for LP)
- **Output swing** $\approx V_{DD} - V_{DSsat3} - V_{GS1} - V_{SG2} - V_{SDsat6}$ (☹ for LV)

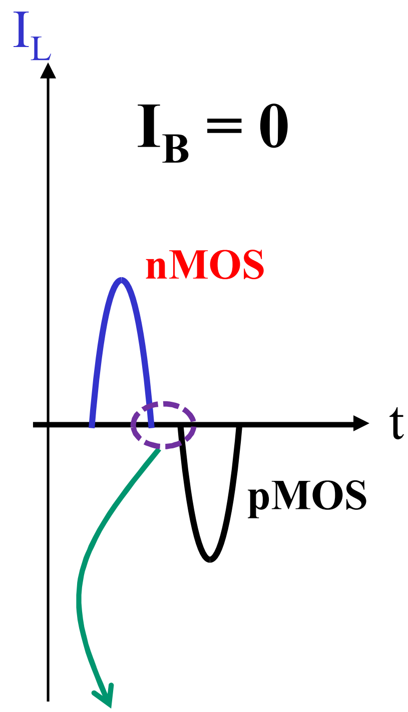
Summary: Class A, B and AB

Class A



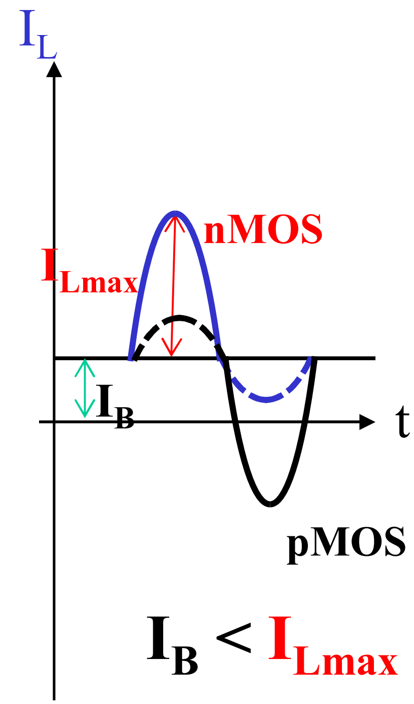
☹ **High power**

Class B



☹ **Crossover Distortion**

Class AB



Lower power
Lower Distortion

Low ΔV_{omax} (LV ☹)

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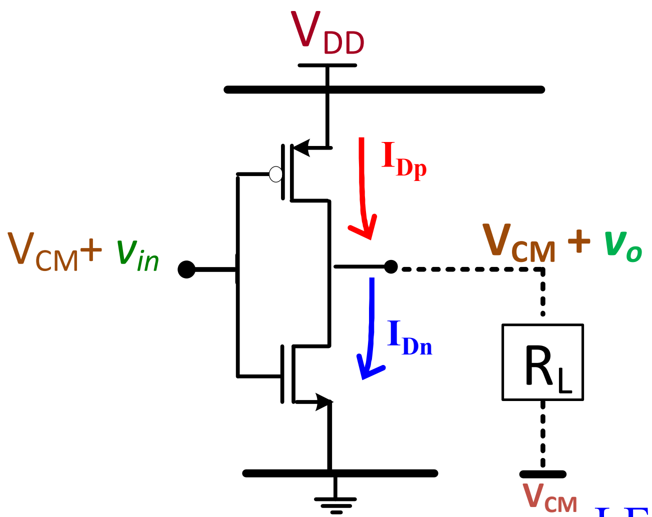
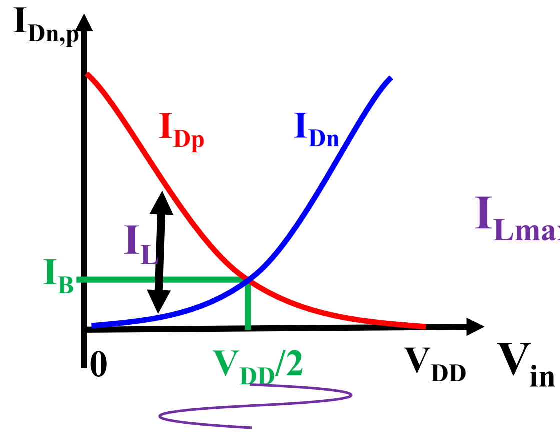
Push-Pull "drain to drain" or "Rail to rail",

Common Source Amplifier: Class AB





$I_{Lmax} >> I_B$

LF Gain with R_L:

$$A_o = -\frac{g_{mn}+g_{mp}}{g_{dsn}+g_{dsp}+R_L^{-1}}$$

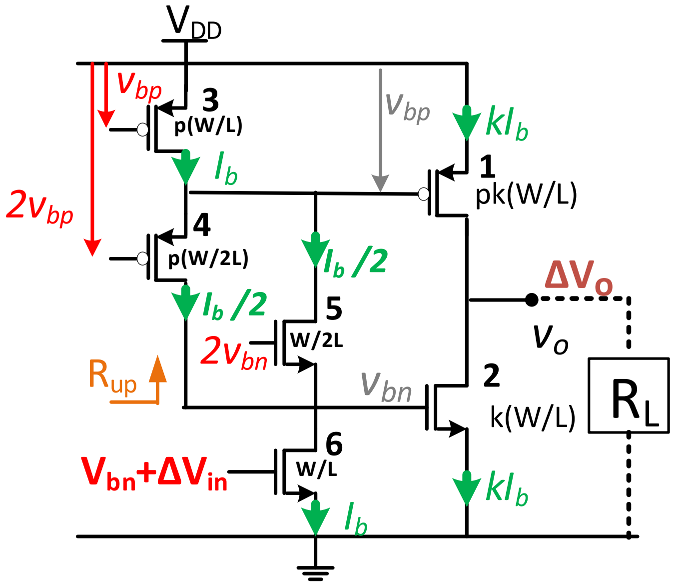
$$\approx -(g_{mn}+g_{mp})R_L \;\; \alpha \; R_L$$

- $V_{OMaX} = V_{DD} - V_{SDsatp}$; $V_{OMin} = V_{DSsatn}$
- Output swing ≈ V_{DD} - $2V_{DSsat}$ (~Rail to Rail) (☺ for LV)
- **Quiescent current corresponds to $V_{in} = V_{out} = V_{CM} = V_{DD}/2$**

→ **Class AB quiescent current = I_B quite small ($I_{Lmax} > I_B$) (☺ for LP)**

- **Weak control of Quiescent current: it depends on the power supply ☹**
- **Weak PSRR ☹**
- **Weak control of design parameters (g_m , gain, GBW …) ☹**

OA Output Buffer: Biasing Class AB "drain to drain" or "Rail to Rail" Buffer using floating current source



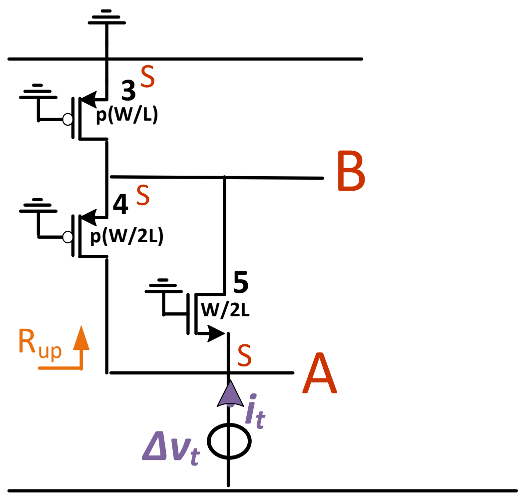
- Transistors 4 and 5 act like a floating current source.
- 6 forms a common-source stage that allows moving the floating current source up and down.
- The sizes and the biasing of 5 and 6 sets V_{gs} of 2 to V_{bn} (rep. the sizes and the biasing of 3 and 4 sets V_{sg} of 1 to V_{bp}) . This makes the **quiescent output current (and so ac parameters) independent on the power supply (GND, V_{DD}) and improves the PSRR ☺☺**
- The dimensioning is usually done for the quiescent condition where the output signal is zero. For this case (3,4)/1 and (5,6)/2 act like current mirrors. The ratio determines the quiescent current.

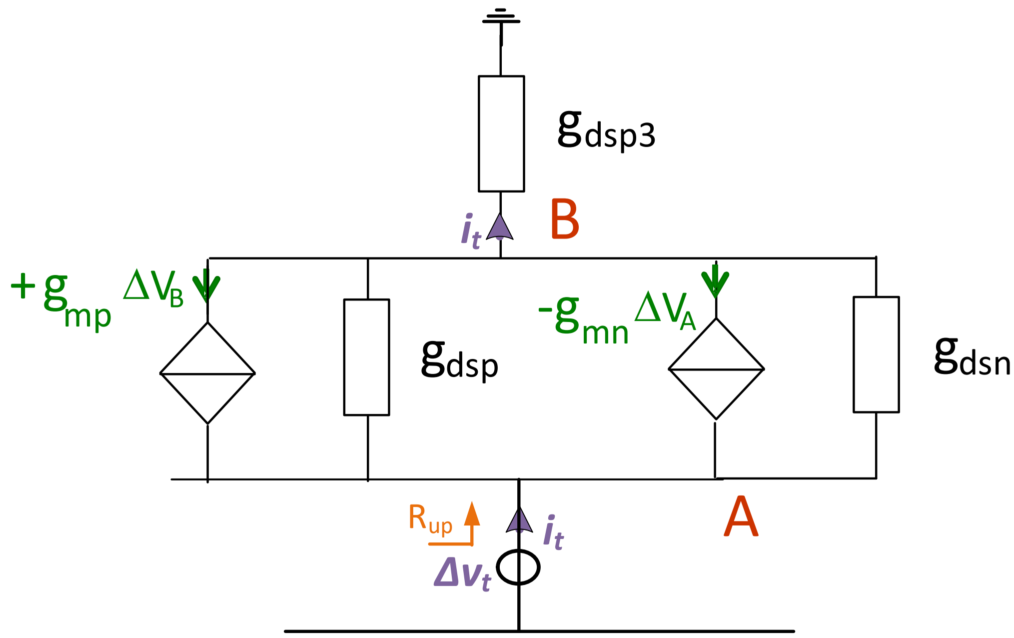
$$R_{up} \approx \frac{1}{g_{ds3}} \quad (if\, g_{m5} = g_{m4})$$

$$A_o \approx \frac{g_{m6}}{g_{ds6}+g_{ds3}} \frac{g_{mn}+g_{mp}}{g_{ds1}+g_{ds2}+R_L^{-1}}$$

☺ Output swing ≈ V_{DD} (Rail to Rail)
☺ Controlled Biasing of the output and high PSRR
☺ Diff to single output by (in+ sur 6 and in- sur 3)

$$R_{up} \approx \frac{1}{g_{ds3}} \quad (if\, g_{mp5} = g_{mn4}) \; ?$$



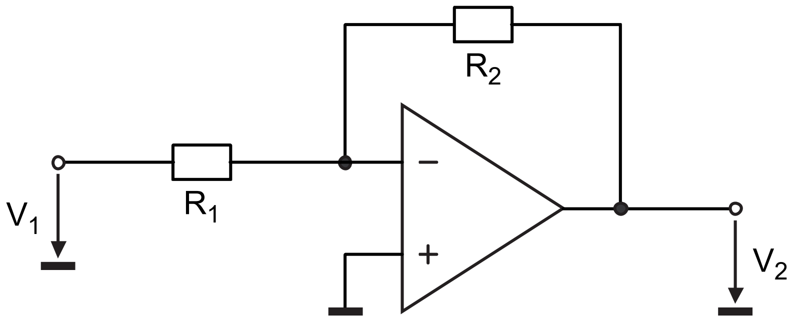


$$i_t = -g_{mp}\frac{i_t}{g_{dsp3}} + g_{mn}\Delta v_t + \left(\Delta v_t - \frac{i_t}{g_{dsp3}}\right)(g_{dsp} + g_{dsn})$$

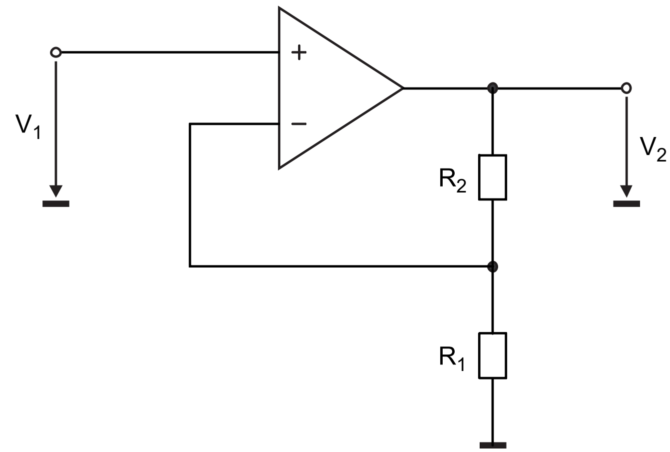
$$R_{up} = \frac{\Delta v_t}{i_t} = \frac{g_{dsp3} + g_{mp} + g_{dsp} + g_{dsn}}{g_{dsp3}\left(g_{mn} + g_{dsp} + g_{dsn}\right)} \xrightarrow{if\, g_{mp} \approx g_{mn}} \frac{1}{g_{dsp3}}$$

Rail to Rail input amplifiers

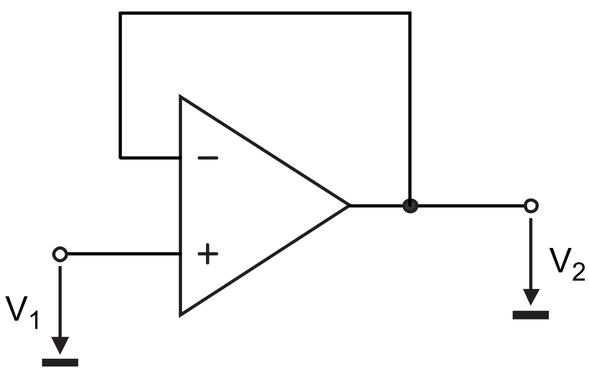
Why Rail-to-Rail input?



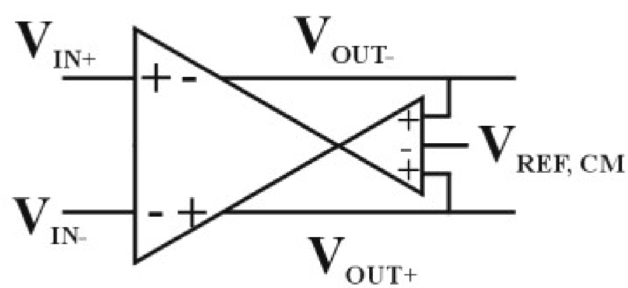
Inv-Amp: No need



Non-In Amp: No need

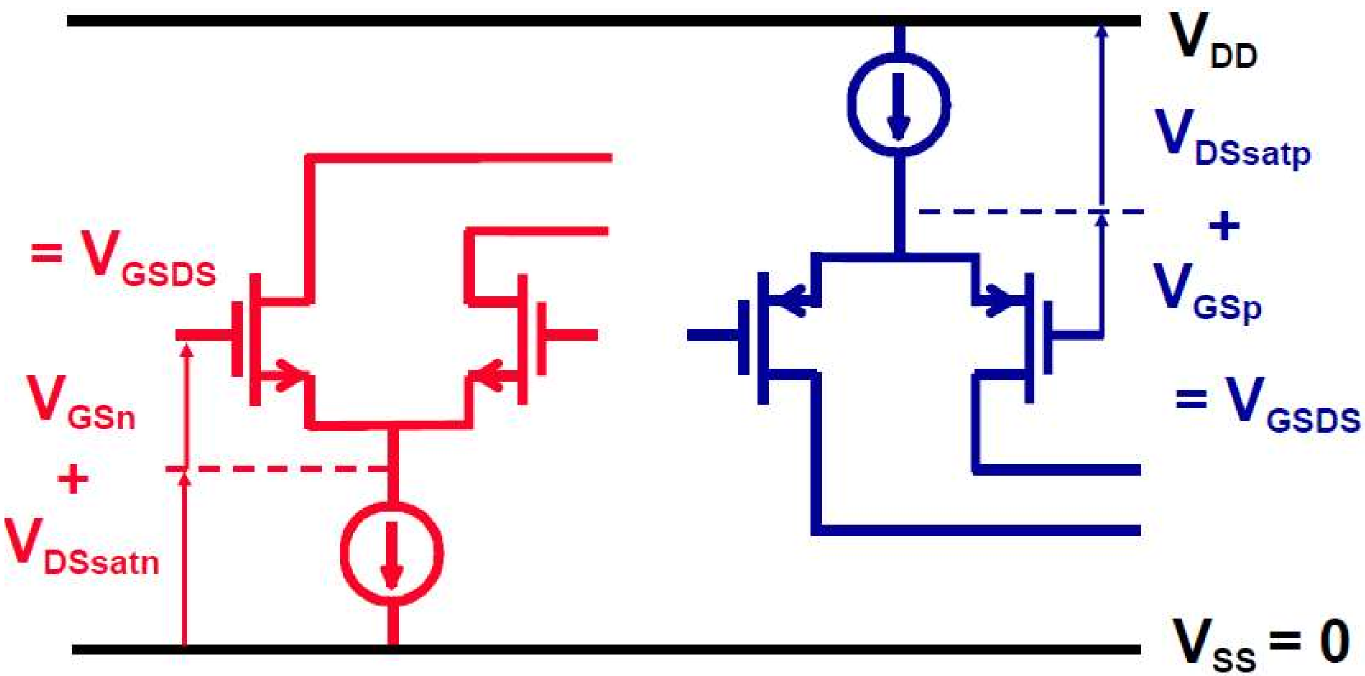


Yes !



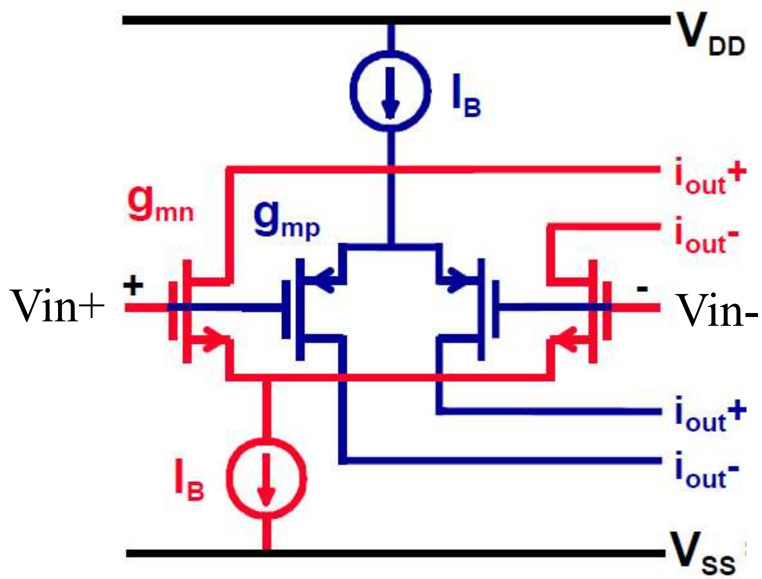
Yes !

nMOS and pMOS input common mode range in Folded-Cascode?



- nMOS : $V_{inCM,min} = V_{GSn} + V_{DSsatn}$ (≈ 0.5 V for $V_{ov} \approx 0.1$ V, $V_T \approx 0.3$ V and $V_{DD} = 1.2$ V)
- pMOS : $V_{inCM,max} = V_{DD} - V_{DSsatp} - V_{GSpn}$ (≈ 0.7) (☹ for LV) .
- Solution: Connect the two complementary pairs in parallel.

nMOS-pMOS input diff. pairs



- Two complementary input pairs in parallel results common-mode input range that exceed the supply rails.
- 3 Operation Areas:
  1. V_{inCM} close to V_{ss}; Only pMOS diff-pair is active.
  2. V_{inCM} close to $(V_{DD} - V_{ss})/2$; both the NMOS and the PMOS diff-pairs will be active.
  3. V_{inCM} close to V_{DD} only nMOS diff-pair is active.
- ☹ Total g_m depends on the common-mode input level.

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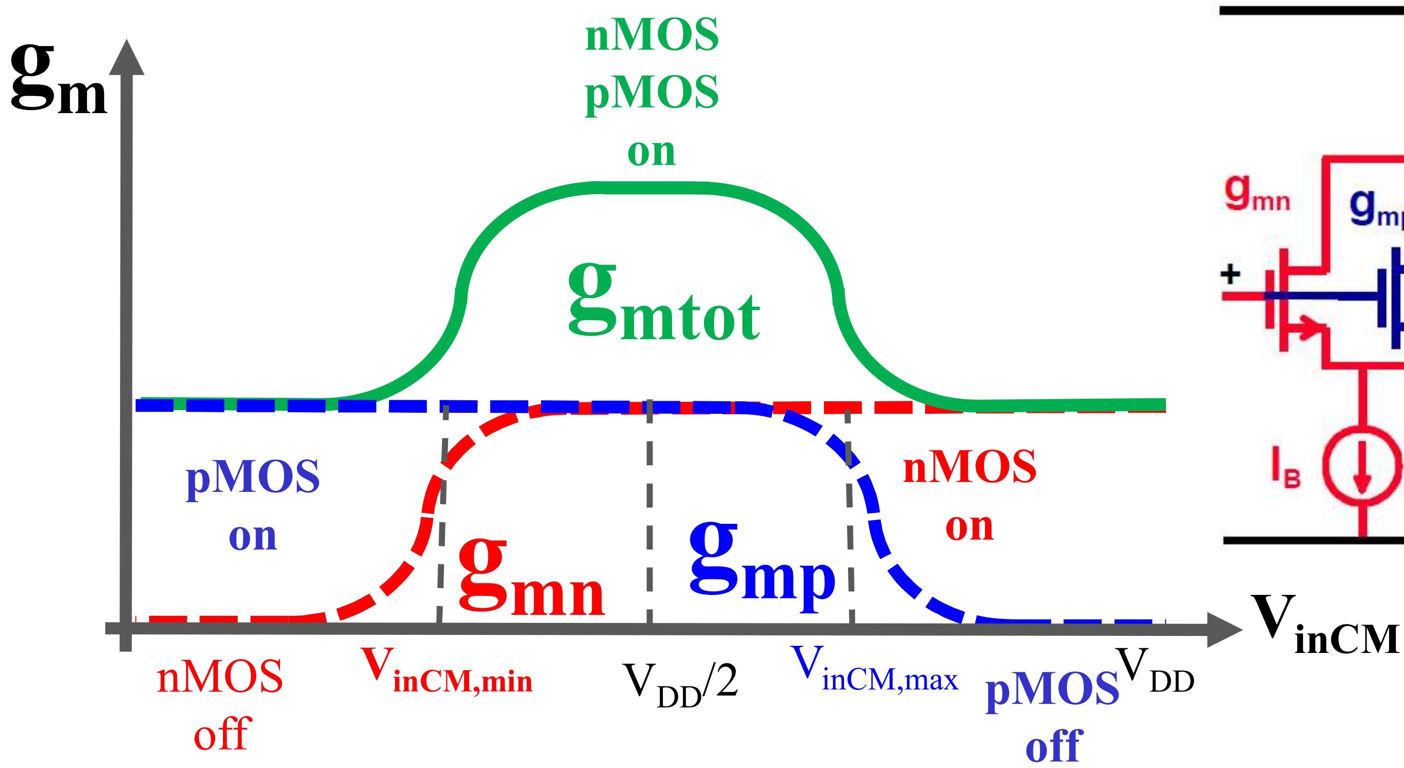
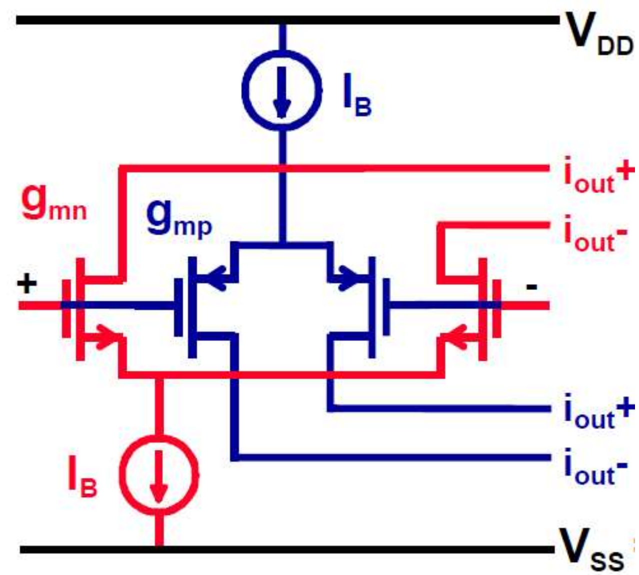
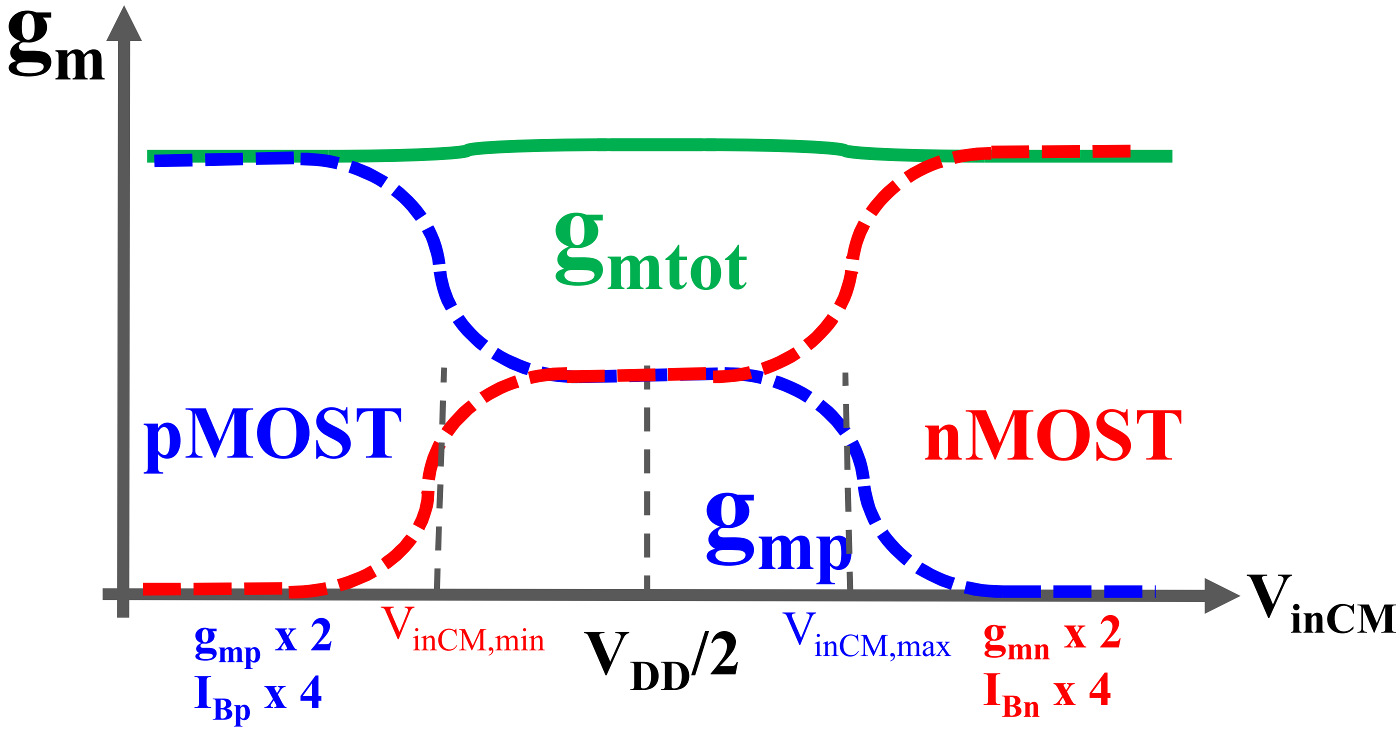
Problem: Unequal g_{mtot}





- ☹ g_m variation → High level of distortion and variation of GBW (stability issue)
- Solution: adjust the tail currents of the differential pairs to equalize $g_{m,tot}$

Rail-to-Rail constant-g_m



- Solution: increase the g_m of each pair by a factor of two at the borders
- In Strong inversion: Double the g_m → Multiply the current by for.

Implementation: Increase the bias current of nMOS by 4 when the bias current of pMOS drops below its nominal value, and vice versa, → add two current mirrors.

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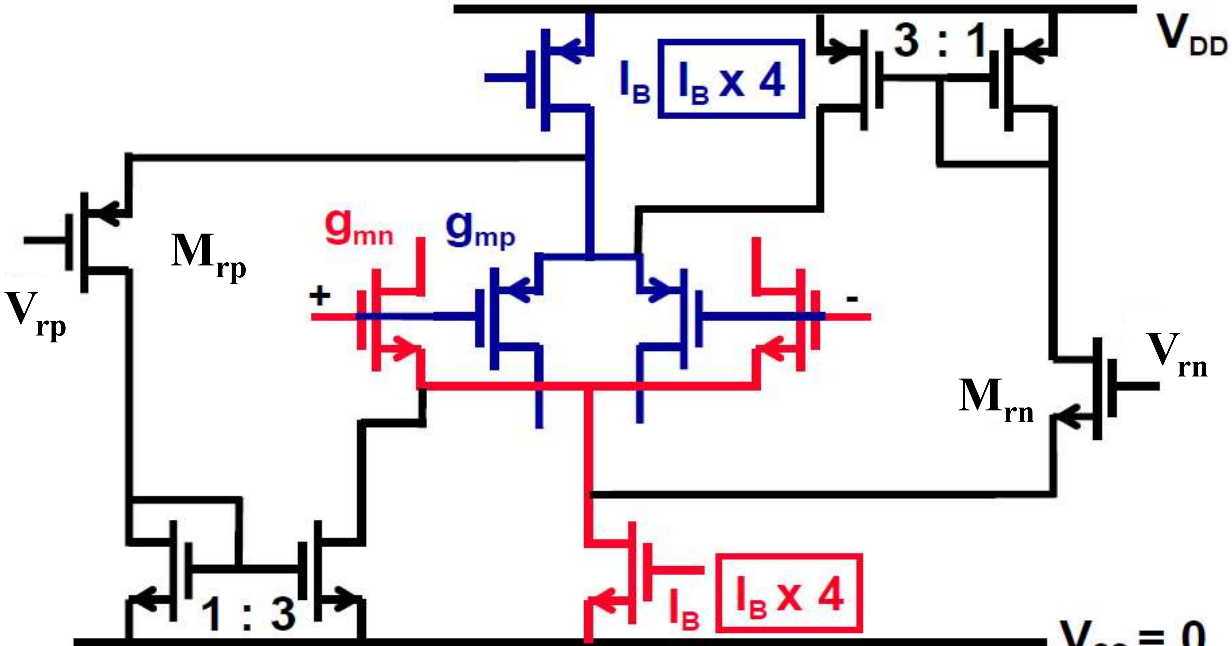
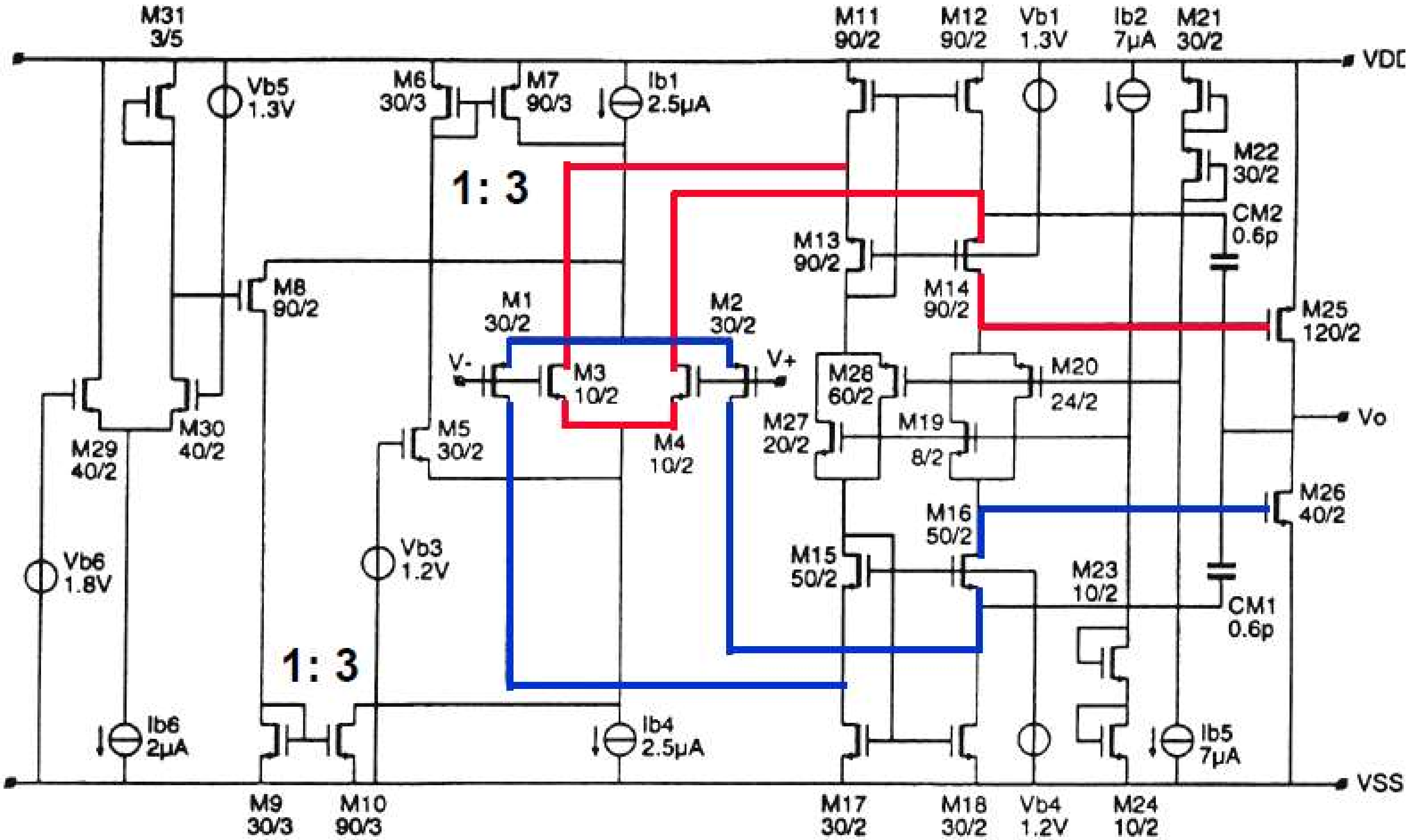
2x current mirror for input biasing



- For $V_{inCM} > V_{inCM,min}$ (nMOS on), $\mathbf{M_{rn}}$ is off
- For $V_{inCM} < V_{inCM,min}$ (nMOS off), $\mathbf{M_{rn}}$ turns on and all current $\mathbf{I_B}$ is pulled through transistor $\mathbf{M_{rn}}$, multiplied by 3 and added to $\mathbf{I_B}$ of the **pMOST pair** (i.e. $\mathbf{I_{Bp}}$ **x 4** → $\mathbf{g_{mp}}$ **x 2**)
- **For** $\mathbf{V_{inCM}} > V_{inCM,max}$ (pMOS off), the opposite operation occurs **(** i.e. $\mathbf{I_{Bn}}$ **x 4** → $\mathbf{g_{mn}}$ **x 2**)
- Transconductance is then equalized over the whole common-mode input range.

Rail to rail input-output Op-Amp



Ref.Hogervorst, JSSC Dec.1994, 1505-1512